WE CLAIM:

1. A method of forming a transistor gate stack, comprising:

forming a high dielectric constant material over a semiconductor substrate;

depositing a silicon-containing seed layer over the high dielectric constant material under seed phase conditions selected to minimize hydrogen reduction of the high dielectric constant material; and

depositing a silicon-containing bulk layer over the seed layer under bulk phase conditions different from the seed phase conditions, the bulk phase conditions selected to result in a higher deposition rate than the seed phase conditions.

2. The method of Claim 1, wherein a deposition rate of the seed phase conditions is less than 500 Å/min and the deposition rate of the bulk phase conditions is greater than 500 Å/min.

3. The method of Claim 2, wherein the deposition rate of the seed phase conditions is between about 10 Å/min and 100 Å/min.

4. The method of Claim 1, wherein the seed phase conditions include a lower temperature than the bulk phase conditions.

5. The method of Claim 1, wherein the seed phase conditions include a lower partial pressure than the bulk phase conditions.

6. The method of Claim 1, wherein the seed phase conditions include supplying a non-hydrogen carrier gas with a silicon source gas.

7. The method of Claim 6, wherein the bulk phase conditions include supplying a non-hydrogen carrier gas with a silicon source gas.

8. The method of Claim 1, wherein the seed layer and the bulk layer form a silicon-germanium gate stack.

9. The method of Claim 1, wherein the bulk layer is *in situ* electrically doped.

10. The method of Claim 1, wherein the seed phase conditions include flowing a higher order silane.

11. The method of Claim 10, wherein the higher order silane comprises disilane.

12. The method of Claim 10, wherein the higher order silane comprises trisilane.

13. The method of Claim 12, wherein depositing comprises heating the substrate to a temperature between about 400°C and 600°C.

14. The method of Claim 10, wherein the partial pressure of the higher order silane in the seed phase conditions is between about 1 mTorr and 1 Torr.

15. The method of Claim 14, wherein the seed phase conditions include flowing an inert, non-hydrogenated carrier gas.

16. The method of Claim 15, wherein the carrier gas comprises nitrogen.

17. The method of Claim 15, wherein the bulk phase conditions also comprise flowing the inert, non-hydrogenated carrier gas.

18. The method of Claim 1, wherein the high dielectric constant material is selected from the group consisting of zirconium oxide, hafnium oxide, tantalum oxide, aluminum oxide, barium strontium titanate, strontium bismuth tantalate, and lanthanide oxides.

19. The method of Claim 18, wherein the high dielectric constant material comprises zirconium oxide.

20. A method of forming a structure in an integrated circuit, comprising:

forming a layer of high dielectric constant material; and

depositing an electrode material over the layer of high dielectric constant material by flowing a higher order silane.

21. The method of Claim 20, wherein the higher order silane comprises trisilane.

22. The method of Claim 21, wherein depositing the electrode material further comprises flowing a germanium source gas.

23. The method of Claim 21, wherein depositing comprises maintaining a reaction chamber pressure between about 1 Torr and 100 Torr.

24. The method of Claim 23, wherein the reaction chamber pressure is maintained between about 10 Torr and 80 Torr.

25. The method of Claim 21, wherein depositing comprises maintaining a substrate temperature between about 300°C and 650°C.

26. The method of Claim 25, wherein the substrate temperature is maintained between about 400°C and 600°C.

27. The method of Claim 26, wherein the substrate temperature is maintained between about 450°C and 575°C.

28. The method of Claim 20, wherein the higher order silane comprises disilane.

29. The method of Claim 20, wherein forming the layer of high dielectric constant material comprises an atomic layer deposition process.

30. The method of Claim 29, wherein the high dielectric constant material is selected from the group consisting of zirconium oxide, hafnium oxide, tantalum oxide, aluminum oxide, barium strontium titanate, strontium bismuth tantalate, and lanthanide oxides.

31. The method of Claim 29, wherein the high dielectric constant material comprises a mixture of metal oxides.

32. The method of Claim 31, wherein the mixture comprises hafnium oxide and aluminum oxide.

33. A method of forming a silicon-containing material over a high dielectric constant material, comprising:

loading a substrate into a single-substrate reaction chamber;

depositing a silicon-containing layer over a high dielectric constant layer on the substrate without flowing hydrogen.

34. The method of Claim 33, wherein depositing comprises a seed phase conducted at a first temperature and a bulk phase conducted at a higher temperature.

35. The method of Claim 34, wherein the seed phase comprises maintaining a temperature of the substrate between about 400°C and 650°C.

36. The method of Claim 33, wherein depositing comprises flowing nitrogen as a carrier gas for a silicon source gas.

37. The method of Claim 37, wherein the silicon source gas comprises silane.

38. The method of Claim 33, wherein depositing comprises flowing a carrier gas comprising a noble gas along with a silicon source gas.

39. The method of Claim 33, wherein depositing comprises maintaining a temperature between about 300°C and 800°C.